IFW

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.: 10/606,283 Confirmation No.: 3304

In re Application of:

Noriko SHINOMIYA Group Art Unit: 2825

Filed: June 26, 2003 Examiner: Nghia M. Doan

For: Semiconductor Integrated Circuit Designing Apparatus, Semiconductor Integrated Circuit Designing Method, Semiconductor Integrated Circuit Manufacturing Method, and Readable Recording Media

REQUEST FOR ACKNOWLEDGMENT OF RECEIPT AND CONSIDERATION OF INFORMATION DISCLOSURE STATEMENT

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Applicants respectfully request the U.S. Patent and Trademark Office to return an initialed copy of the PTO-1449 filed August 7, 2003 with the IDS as acknowledgment of receipt and consideration thereof. A courtesy copy of that PTO-1449, IDS and references filed therewith, as well as a copy of applicants' representatives' postcard receipt evidencing receipt of these documents by the PTO, are enclosed.

Should there be any questions regarding this matter, the appropriate Patent and Trademark Office official is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

STEPTOE & JOHNSON LLP

November 29, 2005
Date

Roger W. Parkhurst
Registration No. 25,177

RWP/ame

Attorney Docket No. 28951.1165

STEPTOE & JOHNSON LLP
1330 Connecticut Avenue, NW
Washington, DC 20036-1795
Tel: (202) 429-6420

OIPE IAP13
NOV 29 2005
PATENT & TRADEMARK OFFICE

Atty. Docket No. HYAE:165

Description: Subm of Orig Ex Decl w/ Ex Decl; Assign Trans Ltr w/ Ex Assign; Clm for Prty w/ cc no. 2002-188421; IDS; PTO-1449; Three (3) Refs; Check No. 16771 ; $2,102.00

OIPE JC14
AUG 07 2003
PATENT & TRADEMARK OFFICE

Inventor(s): ~~Noriko SHINOMIYA~~

Title (new cases):

Attorney: RWP:klb Serial No.: 10/606,283

Paper(s) Filed: August 7, 2003

Date(s) Satisfied: 08/26/03 (MP); 09/26/03 (IDS)

N.D.D.: None

OIPE IAP13
NOV 29 2005
PATENT & TRADEMARK OFFICE

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Noriko SHINOMIYA

Serial No.: 10/606,283 Group Art Unit: Unassigned

Filed: June 26, 2003 Examiner:

For: SEMICONDUCTOR INTEGRATED CIRCUIT DESIGNING APPARATUS, SEMICONDUCTOR INTEGRATED CIRCUIT DESIGNING METHOD, SEMICONDUCTOR INTEGRATED CIRCUIT MANUFACTURING METHOD, AND READABLE RECORDING MEDIA

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Pursuant to 37 C.F.R. §1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached Form PTO-1449. Copies of each of the references listed on Form PTO-1449 are attached.

The above information is presented so that the Patent and Trademark Office may, in the first instance, determine any materiality thereof to the claimed invention. See 37 C.F.R. 1.104(a) and 1.106(b) concerning the PTO duty to consider and use

any such information. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that these references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

Respectfully submitted,

PARKHURST & WENDEL, L.L.P.

August 7, 2003
Date

Roger W. Parkhurst
Registration No. 25,177

RWP/klb

Attorney Docket No.: HYAE:165

PARKHURST & WENDEL, L.L.P.
1421 Prince Street, Suite 210
Alexandria, Virginia 22314-2805
Telephone: (703) 739-0220

Sheet 1 of 1

FORM PTO 1449 (*modified*)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

LIST OF REFERENCES CITED BY APPLICANT(S)
(*Use several sheets if necessary*)

ATTY DOCKET NO. HYAE:165	SERIAL NO. 10/606,283
APPLICANT Noriko SHINOMIYA	
FILING DATE June 26, 2003	GROUP

OIPE
NOV 29 2005
PATENT & TRADEMARK OFFICE

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	2001/0042238 A1	11-15-2001	Hirotaka Ishikawa	716	10	12-27-2000

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION NO	TRANSLATION YES
	2000-208634 A	07-28-2000	Japan				Abstract

OTHER DOCUMENT(S) (*Including Author, Title, Date, Pertinent Pages, Etc.*)

	CHEN, Howard H., et al., "Power Supply Noise Analysis Methodology for Deep-Submicron VLSI Chip Design", IBM Research Division, Thomas J. Watson Research Center, Yorktown Heights, NY 10598, U.S.A., pages 638-643.

EXAMINER: DATE CONSIDERED:

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.